

### **Now-5/03 President & Owner / Alpine IC Innovations, LLC, Ft. Collins, CO**

Alpine offers custom contract analog IC design and layout services. Alpine also designs and markets IP cores for low-power, low-voltage, area-efficient using CMOS, BiCMOS, or Bipolar processes. IP core blocks of emphasis are 10-12bit IQ ADCs, DACs, PLL's, and other circuits commonly used in wireless and network communications. Alpine's design and layout areas have been in the following areas.

- Analog to Digital Converters (ADCs) (pipeline, SAR, sigma-delta)
- Digital to Analog Converters (DACs) (video, current steering, switch-capacitor)
- Low-Noise Amplifiers (LNA), Variable Gain Control (VGA), Mixers for RF and Wireless Applications
- Low-Noise Low-Distortion Amplifiers (LNA) for Ultra-Sound and Imaging
- Low-Noise Low-Distortion Amplifiers (LNA) for piezo-electric capacitive sensors
- Low-Noise Low-Distortion Amplifiers (LNA) for MEMs applications with very low noise 1/f component
- Low-Noise Low-Distortion MEMs audio detection circuits
- Low-Noise DACs for Ultra-Sound Imaging Transmit
- Low phase noise LC Oscillators
- 1.2V and sub 1V Bandgap Voltage & Current References

### **8/02-5/03 Staff Analog IC Design Engineer / Airgo Networks, Ft. Collins, CO**

Full-custom CMOS and BiCMOS analog design TSMC0.13u and IBM Sige5am RF processes including design, layout, and all verification. Designs included:

- 10-b 40/80MS/s 55mW 3v Pipeline ADC with > 100 MHz BW for 802.11 WLAN
- 7 GHz RF clock synthesis circuits for 802.11 WLAN RF Front End IC
- Power-On Reset for 802.11 WLAN RF Front End IC
- RC Receive Filter With Automatic PVT Tuning for 802.11 WLAN RF Front End IC
- 1.2 V CMOS Very-Low-Jitter Clock Source Multiplier For ADC Clock
- 80 MSPS CMOS IQ transmit DAC
- Top-Level Analog Super Block Layout and Verification

Lead analog IC design engineer in remote Colorado office of Wireless LAN start up company Palo Alto, CA. Given responsibility for all CMOS base-band CMOS analog circuits including IQ ADC/DAC, PLL, ADC clock source multiplier, and housekeeping ADCs. Participated in two RF front-end chip developments in Bi-CMOS. Responsible for all tools setup and maintenance for Colorado site.

### **4/98-8/02 Principal Analog IC Design Engineer / Philips Semiconductors, Ft. Collins**

Full-custom CMOS analog design, layout, verification, customer interface, quotes and feasibility studies, die area, resource and cost estimates. Projects include:

- 100-MS/s 10-b, 13-pA/rtHz 50-mW Low Noise DAC for Ultrasound Imaging
- 10-b 80MS/s 80mW 2.5v Pipeline ADC with > 100 MHz BW for 802.11 WLAN
- 6-GHz Low Skew, CMOS Single-Ended-to-Differential Converter Without Static Power Dissipation
- 3.2-Gbps 3.4-mW 32-pS Skew CMOS Receiver for LVDS
- 3.2-Gbps 19-mW 15-pS Skew CMOS LVDS Transmitter
- 90 MS/s 65mW 2.5V 8-b Pipeline ADC with > 100 MHz BW for 802.11/Bluetooth WLAN
- LAN/WAN LonWorks Transceiver for Coactive Networks
- QPSK Transmit DAC and Gm-C Continuous Time Reconstruction Filter for 802.11 WLAN
- 10b SAR ADC INL Calibration Circuit
- HDTV Color Decode Custom Analog Digitizer including 5-10b video ADCs and 4 DACs.
- Automatically Tuned Video RC Anti-Alias Filter Circuits over Process Voltage and Temperature

*All silicon first-pass successful to specification.* Lead technical contributor for satellite design office. Promoted from Staff to Principal Engineer. Awarded one of few special retention incentives for Philips North America. Responsible for co-developing front and backend tool flow and design methodology for a small design office as well as system administration. Instrumental in recruiting to grow the group from 2 original to 6 employees.

#### **7/96-4/98 Analog IC Design Engineer / Hewlett-Packard, Fort Collins, CO**

Responsible for all analog transistor level design of HP's 3.3V CMOS Optical Navigation Imaging IC for hand-held free-space pointer. This technology is now used in all of the light based mice for Logitech and Microsoft. Responsible for design of photo-receivers, switched capacitor charge amplifiers, ADC, bias and pad cells.

Designed 3.3V all CMOS single supply low noise MR preamplifier featuring 8 simultaneous read/write channels, noise figure < 3 dB, BW > 100 MHz, bi-directional bias current DAC control, thermal asperity detection and read/write fault detection. Write current driver feature 4 ns rise/fall times with programmable current. Responsible for RFQ responses, feasibility analysis of ASICs and customer presentations. Investigations included design for 7 pole gm-C equalization filter for PRML read channel.

#### **4/92-7/96 Read-Write Preamp IC Design Engineer / Hewlett-Packard, Boise Idaho**

Co-developed with Philips Semiconductors the world's first dual-stripe magneto-resistive (MR) preamplifiers. All chips first pass functional and resulted in 3 generations of high-speed low-noise dual-stripe MR, preamps for hard disk drives starting with the miniature 1.3" Kittyhawk HDD, to the high data rate Cougar II at 18 GB, 200+ Mb/S. These preamps revolutionized the high-end preamplifier market with the highest data rates, fastest write characteristics and lowest noise figure of the industry. Co-developed on-chip MR-bias and write current programming via on-chip DACs and 3-wire serial interface, original features which quickly became the industry standard.

Preamp development responsibilities included chip architecture, specifications, testing, modeling, measurement, optimization of thermal characteristics and impedance matching of head-preamp-channel interconnect. Solely performed all preamplifier characterization including all testing over temperature and process extremes to ensure production ready status. Responsible for all MR flex circuit, head-stack-assembly (HSA), preamplifier electrical design and characterization. Developed all characterization software to control spectrum & network analyzers and oscilloscopes to create fully automated and flexible test environments. Designed Cougar II production HSA tester. Provided critical electronics support for head-media, channel, mechanical flex circuit and process engineers which enabled success of HP's DSMR head technology invention. Co-developed all-surface formatting.

Proficient in high frequency PCA design including ECL, PECL, custom active probes, TDR, transmission line, and very low-noise amplifier design and measurement. Designed worlds fastest (at the time) differential probe (> 600 MHz BW) for preamp and read-channel characterization. Designed 5 Altera Field-Programmable-Gate-Arrays. Co-engineered and characterized accelerometer ICs for HP's shock resistant portable Kittyhawk.

#### **4/88-4/92 Principal Design Engineer / Honeywell, VLSI Division, Phoenix, AZ**

Promoted from Senior Project Engineer to Principal Engineer. The CTO VLSI Design Division provides centralized ASIC design support for Honeywell. Designers enjoy a large variety of circuit and system applications using multiple foundries. Provided design services for both bipolar and CMOS technologies. Solely responsible for all phases of ASIC development including requesting foundry quotes, foundry selection, design & simulation, layout, characterization, foundry interface, customer interface.

Designed first pass successful video processor. Design proficiency in gain-controlled amplifiers, multipliers, transimpedance amplifiers, precision gain and offset and control interface. Designed first pass successful ARINC 429 transmitter now flying in Boeing 737, 747, 767, 777. Designed light-intensity-servo-control and thermo-electric-cooler-control ICs for Honeywell's Fiber Optic Gyro, both first-time successes. Provided design and consulting for many other ASICs. Cell development for ADC, DAC high speed and high power op-amps, low noise preamplifiers, sample-holds, phase detectors, VCOs power FET driver, voltage regulators and bandgap references.

Responsible for circuit design in Honeywell's first commercially available Fiber Optic Gyro. Circuit design responsibilities included low noise transimpedance amplifiers, precision mixers, synchronous demodulators, active and passive filters, ultra-low distortion signal generators (< 120 dB), digital ASIC interface, high speed signal synchronization, and custom 20-bit ADC for on-chip altimeters.

### **3/89-11/89 Senior Analog Design Engineer / Areal Technology Inc, Tucson, AZ**

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As one of 5 engineers in the R&D startup, designed all head positioning servo hardware and seek algorithm for Areal Technology's 3.5" HDD. Areas of design responsibility included read/write data channel, low noise preamplifiers, head positioning and servo control electronics, actuator amplifiers in addition to mechanical issues of resonance suppression and vibrational analysis. Developed non-linear behavioral model of head positioning servo and seek algorithm for new seek method.

### **9/86-4/88 Disk Drive Servo Design Engineer / Iomega, R& D Laboratory, Roy, UT**

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Designed interferometer based head positioning electronics for disk drive servo writers. Developed head positioning electronics for 3.5" Gamma removable storage drive. Design responsibilities include feedback and control systems, PLLs, filtering and noise reduction, magnetics and laboratory measurements of electromechanical devices.

## ***Education and Honors***

**MSEE Yale University 1986.** Honors grade average.

**BSEE University of Utah 1985.** Minor: physics. Magna Cum Laude.

- Elected member and officer of **Tau Beta Pi** and **Eta Kappa Nu** Honor Societies.
- Awarded, by Yale University, Ph.D. fellowship for tuition and stipend.
- Recipient of cash technical achievement award for low distortion achievements on Honeywell's Fiber Optic Gyro now flying in Boeing 777.
- Two patents applied for on modulation index servo control method for fiber optic gyros.

## ***Patents Awarded***

- **Circuit and Method for Testing a Disk Drive Assembly Without Probing**, US Patent 5589777, Dec. 31 1996, B. Davis, J. O. Voorman, N. V. L. Ramalho, P. Gamand
- **Magneto-Resistive Head Read Amplifier**, US Patent 6331921 B1, Dec. 18 2001, B. Davis, B. Thelen
- **Programmable Write Driver Circuit for Writing Information to a Magnetic Storage Media**, US Patent 6246533 B1, Jun.12 2001, B. Davis, R. Thelen
- **Scanning Mouse for a Computer System**, US Patent 5994710, Nov. 30, 1999, B. Davis, D. Knee
- **Circuit for Automatically Tuning Filter Circuits over Process Voltage and Temperature**, US Patent 6417727, July 9, 2002, B. Davis
- **Method and Circuit for Automatically Tuning Filter Circuits over Process Voltage and Temperature**, European Patent EP1163720 Dec. 19 2001, B. Davis

## ***Publications & Patents In Progress***

- **A 6-GHz Low Skew, CMOS Single-Ended-to-Differential Converter Without Static Power Dissipation**, May 5 2002, Brad Davis
- **A 3.2-Gbps 3.4-mW 32-pS Skew CMOS Receiver for LVDS**, May 5 2002, B. Davis, F. Creed
- **A 3.2-Gbps 19-mW 15-pS Skew CMOS LVDS Transmitter**, May 5 2002, B. Davis, R. Jansons, B. Woodside

## ***Programming and Computer Skills***

Cadence SpectreRF, Ocean, Lisp, SpectreHDL, Virtuoso Layout, Calibre DRC/LVS, Hspice and Hercules, C, Verilog, VHDL, Unix, Perl, Awk, GPIB instrument control. AHDL field programmable gate array synthesis, OrCAD, Pspice, Mathcad, Matlab, assembly language.